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Design of 60-GHz Millimeter-wave CMOS RFIC-on-Chip CPW-Fed Slot Antenna

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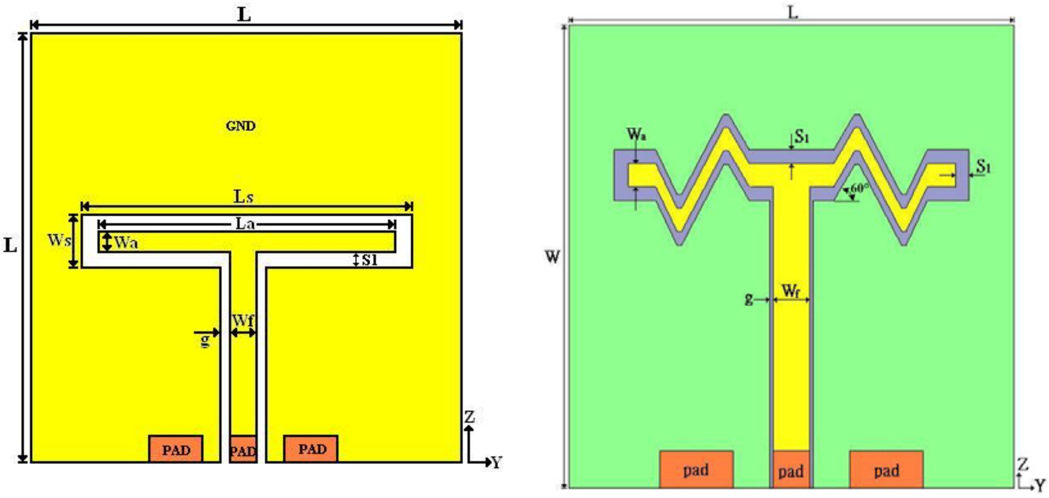
1. Introduction

Recently, there exists an increasing demand for broadband multimedia applications for an ever-increasing capacity of wireless networks. In particular, for dense local communications, the 60-GHz band for wireless personal area network (WPAN) applications is of special interest to the short range communications due to its attenuation characteristic of atmospheric oxygen of 10 to 15 dB/km in a bandwidth of about 8 GHz centered around 60 GHz. It makes the 60-GHz band becomes an attractive alternative for the short-range wireless communications [1]. In order to pursue the RF system-on-chip (SoC) for the 60-GHz radio and the antenna integrated with low-cost monolithically integrated CMOS RF front-end circuitry, millimeter-wave CMOS RFICs and on-chip antenna have been studied [2-4]. In this paper, a 60-GHz CMOS RFIC-on-chip slot antenna is presented. The on-chip antenna is fabricated with a 0.18-μm CMOS process. A rectangular-shaped aperture fed by the CPW line with an exciting stub is adopted to design the RFIC-on-chip antenna. The HFSS FEM-based 3-D full-wave EM solver is used for the design simulation.

2. Antenna Design

Fig. 1 shows the geometries of the designed 60-GHz CMOS CPW-fed RFIC-on-chip slot antenna with the T-shaped and zigzag-shaped stubs. A rectangular aperture is etched out from the ground plane, and a 50-Ω CPW line with an exciting stub is employed to feed the slot antenna [5]. In general, there has several ways to enhance the bandwidth of the slot antenna [6]. One way is to use a widened slot and a stub for excitation. By properly selecting the configurations and the dimensions of the stub, a good impedance matching can be achieved. In this paper, two different shapes are considered: the T- and zigzag-shaped stubs. The T-shaped tuning stub features a low-profile configuration, and the zigzag-shaped tuning stub exhibits a miniaturized dimension as compared to the T-shaped one. Both of the designed 60-GHz CMOS RFIC-on-chip antennas have a performance of wide bandwidth and an omni-directional radiation pattern.

ISBN: 978-4-88552-223-9 C3055©IEICE

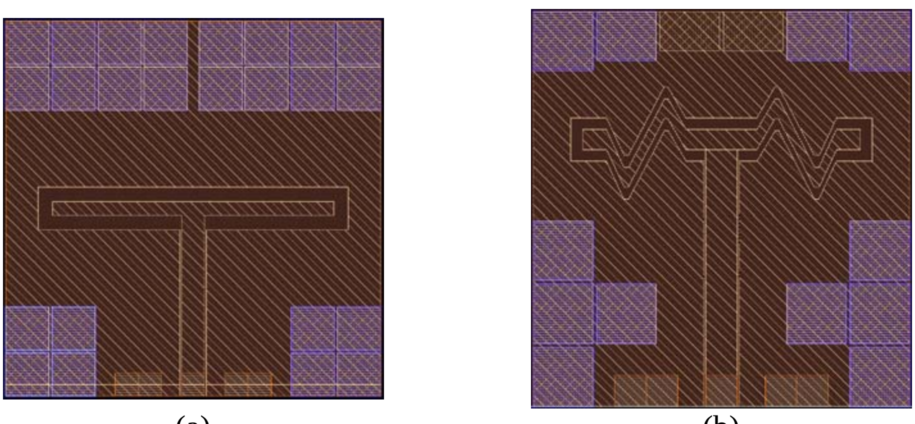


(a) (b)

Fig. 1. Schematics of the designed 60-GHz CPW-fed slot CMOS RFIC-on-chip antenna with: (a) the T-shaped stub and (b) the zigzag-shaped stub.

3. Simulation and Measurement Results

Fig. 2 shows the chip layout of the designed 60-GHz CMOS RFIC-on-chip antenna. The chip sizes of the slot antenna with the T-shaped and zigzag-shaped stubs are 1.3 × 1.3 and 1.00 × 0.95 mm^2, respectively. Fig. 3 shows the simulated input VSWR of the CMOS antenna with the T-shaped and zigzag-shaped stubs, which are less than 2 from 55 to 65 GHz. The simulated antenna radiation efficiencies are about 21 and 13 %, respectively, which may be due to the CMOS substrate loss. The H-plane pattern, as shown in Fig. 4 and Fig. 5, is nearly an omni-directional pattern. For the RFIC-on-chip slot antenna with the T-shaped stub, the simulated maximum, minimum, and average power gain in the H-plane is about -3.6, -8.6, and -6.1 dB, respectively. And the slot antenna with the zigzag-shaped stub, the simulated maximum, minimum, and average power gain in the H-plane is about -6, -10, and -8 dB, respectively. Table I shows the performance summary of the antenna radiation characteristics.



(a) (b)

Fig. 2. CMOS chip layout of the designed 60-GHz CPW-fed slot RFIC-on-chip antenna with: (a) the T-shaped stub and (b) the zigzag-shaped stub.

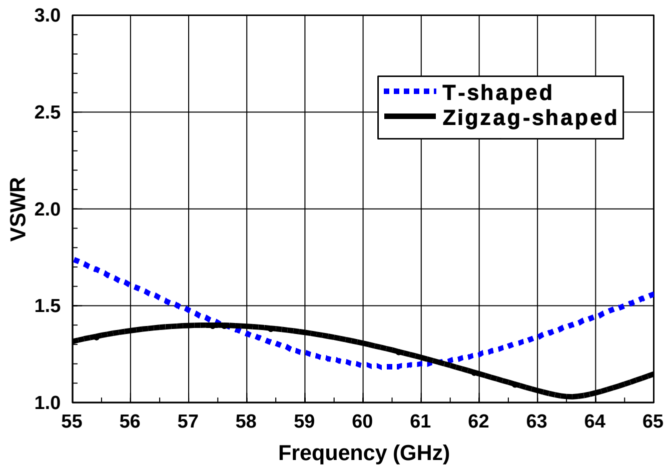
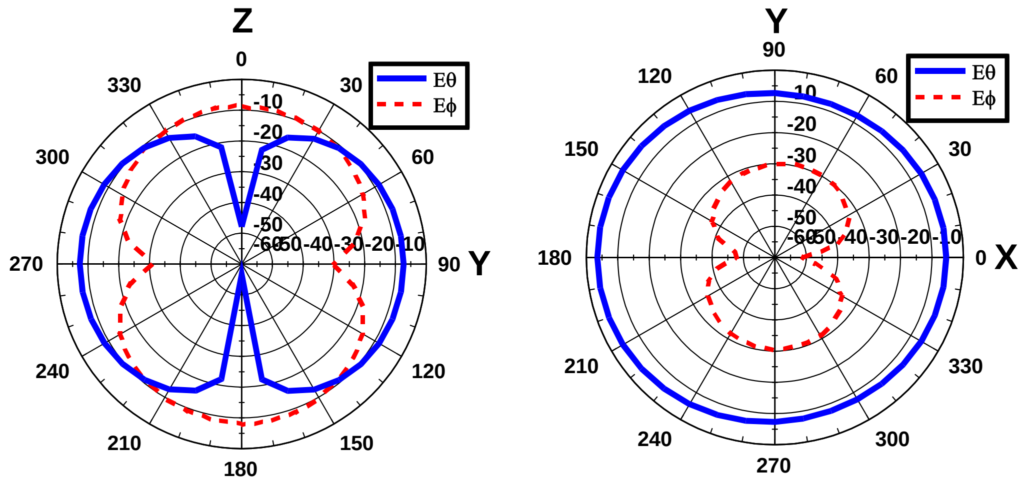
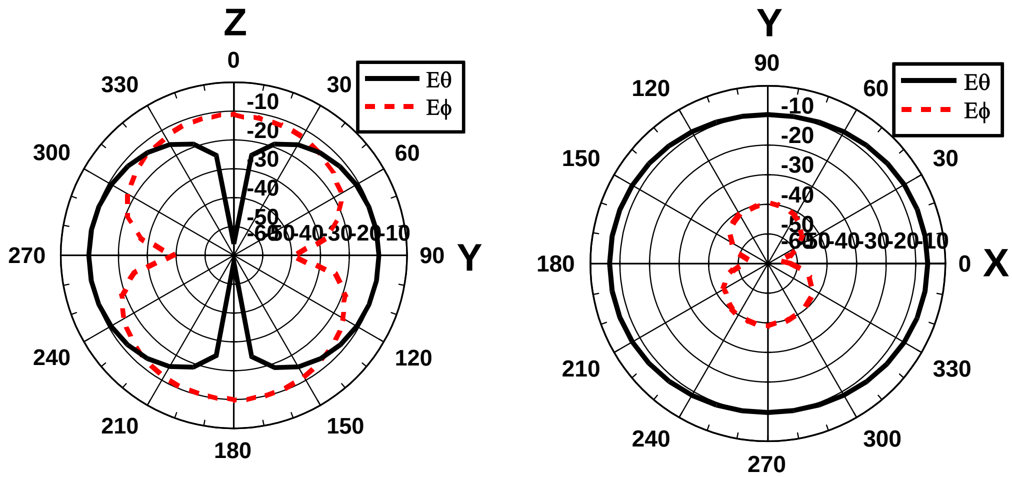


Fig. 3. The HFSS simulated VSWR.



(a) (b)

Fig. 4. HFSS simulated radiation patterns of the CPW-fed slot RFIC-on-chip antenna with the T-shaped stub: (a) E-plane and (b) H-plane.



(a) (b)

Fig. 5. HFSS simulated radiation patterns of the CPW-fed slot RFIC-on-chip antenna with the zigzag-shaped stub: (a) E-plane and (b) H-plane.

Table 1 Simulated Antenna Performance Summary

60-GHz CMOS Antenna	T-shaped stub	Zigzag-shaped stub
Impedance Bandwidth (VSWR<2)	55 - 65 GHz	55 - 65 GHz
Radiation efficiency (η_r)	21 %	13 %
Max. gain in *xy*-plane	-3.6 dB	-6.0 dB

4. Conclusion

This paper presented design of 60-GHz millimeter-wave CMOS RFIC-on-chip CPW-fed slot antenna fro 60-GHz WPAN CMOS transceiver application. The CMOS on-chip antenna is fabricated with a 0.18-μm CMOS process. The HFSS FEM-based 3-D full-wave EM solver is used for the design simulation. A rectangular-shaped aperture fed by the CPW line with an exciting stub is adopted to design the on-chip antenna for wide bandwidth performance. The antennas of two different shapes, the T- and zigzag-shaped stubs with a chip sizes of 1.3×1.3 and 1.00×0.95 mm^2, are designed. The simulated antenna input VSWRs are less than 2 from 55 to 65 GHz and the simulated antenna radiation efficiencies are about 21 and 13 %, respectively, which may be due to the CMOS substrate loss. The H-plane antenna patterns are nearly an omni-directional. The average antenna power gains in the H-plane are about -6.1 and -8 dB for the antenna with the T- and zigzag-shaped stubs, respectively. The developed CMOS on-chip can be used fro the integration of a 60-GHz CMOS single-chip transceiver.

Acknowledgments

The authors would like to thank the Chip Implementation Center (CIC) of the National Science Council, Taiwan, ROC, for supporting the TSMC CMOS process.

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