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1. Introduction

Accurate characterization of field effect transistor (FET) is necessary for precise design of monolithic-microwave integrated-circuit (MMIC). Extraction of FET parameters, or characterization, is difficult because the FET is embedded in the parasitic circuit, which is referred to as test element group (TEG), to connect probe and bias. De-embedding method using open/short-TEG [1] had been widely used in the characterization of FET. But two approximations are used in the de-embedding method using open/short-TEG [1]; (1) incompleteness of open and short pattern, and (2) approximation of a parasitic circuit by an equivalent circuit topology. Those approximations cause ambiguity and non-negligible error especially in high microwave band. So, the authors have proposed the de-embedding method using EM simulator [2], which is more accurate than the conventional de-embedding method.

In this paper, the error factor in the conventional de-embedding method is identified by comparing with the proposed de-embedding method. And, the applicability of the proposed de-embedding method for a coplanar-type TEG with very lossy substrate is investigated because the FET characterization on Si CMOS is very serious problem in the millimeter-wave band.

2. De-Embedding Method Using EM Simulator

Figure 1 shows the de-embedding method using EM simulator; especially FEM-based simulator Ansoft HFSS Ver.9 is used throughout this paper.

(1) Prepare the device with a parasitic circuit.

(2) Analyze S-parameters of the four-port parasitic circuit $S_{(PC)}$ by adding lumped ports, with arbitrary internal impedances, at the terminals of lumped ports: Port3 ($Z_3$ ) and Port4 ($Z_4$). 
Terminals Port1 and Port2 at the parasitic circuit, which are connected to VNA, are normally treated as wave ports.

(3) Measure the S-parameters of the parasitic circuit with the lumped element $S_{(DUT)}$. Conventional calibration methods such as open-short-load (OSL) and/or thru-reflect-line (TRL) can be used for Port1 and Port2 in the measurement using VNA.

(4) Transform $S_{(PC)}$ into hybrid S/Z-parameters $A_{(PC)}$.

$$
\begin{bmatrix}
    \mathbf{b}_a \\
    \mathbf{V}_b
\end{bmatrix} = \begin{bmatrix}
    \mathbf{a}_a \\
    \mathbf{I}_b
\end{bmatrix} = \begin{bmatrix}
    A_{(PC)}^{11} & A_{(PC)}^{12} \\
    A_{(PC)}^{21} & A_{(PC)}^{22}
\end{bmatrix} \begin{bmatrix}
    \mathbf{a}_a \\
    \mathbf{I}_b
\end{bmatrix} = \begin{bmatrix}
    A_{(PC)}^{11} \mathbf{a}_a + A_{(PC)}^{12} \mathbf{I}_b \\
    A_{(PC)}^{21} \mathbf{a}_a + A_{(PC)}^{22} \mathbf{I}_b
\end{bmatrix}
$$

(1)

where, $\mathbf{b}_a = [b_i, b_i]$, $\mathbf{a}_a = [a_i, a_i]$, $\mathbf{V}_b = [V', V']$, $\mathbf{I}_b = [I_j, I_j]$. $A_{(PC)}^{ij}$ are sub-matrices of $A_{(PC)}$, and they can be calculated as follows.
\[
\begin{aligned}
A_{(11)}^{(PC)} &= S_{(11)}^{(PC)} + S_{(12)}^{(PC)}(I - S_{(22)}^{(PC)})^{-1}S_{(21)}^{(PC)} \\
A_{(12)}^{(PC)} &= S_{(12)}^{(PC)}[(I - S_{(22)}^{(PC)})^{-1}(I + S_{(22)}^{(PC)}) + I]\text{diag}([\sqrt{Z_{(1)}^{(PC)}}]/2 \\
A_{(21)}^{(PC)} &= 2\text{diag}([\sqrt{Z_{(2)}^{(PC)}}])I - S_{(22)}^{(PC)})^{-1}S_{(21)}^{(PC)} \\
A_{(22)}^{(PC)} &= \text{diag}([\sqrt{Z_{(2)}^{(PC)}}](I - S_{(22)}^{(PC)})^{-1}S_{(22)}^{(PC)} \text{diag}([\sqrt{Z_{(2)}^{(PC)}}])
\end{aligned}
\]

where \( I \) is an identity matrix, and \( \text{diag}([\sqrt{Z_{(j)}^{(PC)}}]) = \text{diag}([\sqrt{Z_{j}}, \sqrt{Z_{+}}] \) is a diagonal matrix with square root of internal impedances for lumped ports Port3 and 4. \( A_{(11)}^{(PC)} \) has a dimension of S-parameters for Port1 and 2, and \( A_{(22)}^{(PC)} \) has a dimension of Z-parameters for Port3 and 4. Finally, Z-parameters for the embedded lumped device \( Z^{(DEV)} \) can be obtained using terminal condition \( V_y = -Z^{(DEV)} I_x \) and measured S-parameters using VNA \( b_x = S^{(DUT)} a_y \) together with Eq.(1).

\[
Z^{(DEV)} = -A_{(21)}^{(PC)}(S^{(DUT)} - A_{(11)}^{(PC)})^{-1}A_{(12)}^{(PC)} - A_{(22)}^{(PC)}
\]  

3. Numerical Results

Figure 2 shows the structure of a TEG considered in the paper. Port1 and Port2 in Fig.2 (a) are the coplanar waveguide (CPW) with characteristic impedance of 50 \( \Omega \). Two FETs with the same characteristic will be embedded in the TEG. Figure 2 (b) and (c) show open and short pattern for conventional de-embedding method [1], respectively.

The proposed de-embedding method described in section 2 is demonstrated fully-numerically. Figure 3 (a) and (b) show HFSS models for the parasitic circuit and FET-TEG, respectively. Because of the symmetry of the structure and excitation, a half of the whole structure is enough to model with a magnetic wall, or Perfect H in HFSS, at the symmetrical place. Terminals of the transmission line are modelled as wave ports, and terminals for a lumped device are modelled as lumped ports in Fig.3 (a), resulting in \( 4 \times 4 \) S-matrix \( S^{(PC)} \). Given lumped impedances are specified as shown in Fig.3 (b) to simulate measured S-matrix in Step 3 in section 2, resulting in \( 2 \times 2 \) S-matrix \( S^{(DUT)} \). 50 \( \Omega \) and 0.1pF are connected in parallel at the position of LumpedPort1 in Fig.3 (a), while 75 \( \Omega \) and 1nH are connected in parallel at the position of LumpedPort2.

Figure 4 shows the result of numerical simulation of de-embedding when \( \sigma = 0 \). It is observed that the result of the proposed method (solid curve) has higher accuracy than that of the conventional method (dotted curve). In order to identify the error factor in the conventional method, the ideal characteristic of open/short-TEG calculated by the S-parameter of the four port parasitic circuit is used in the conventional method. For S-parameters of ideal open and short-TEG, \( S^{(open)} = A_{(11)}^{(PC)} \) and \( S^{(short)} = A_{(11)}^{(PC)} - A_{(12)}^{(PC)} A_{(22)}^{(PC)}^{-1}A_{(21)}^{(PC)} \) are used, respectively, because solving Eq.(3) for \( S^{(DUT)} \) becomes \( S^{(DUT)} = A_{(11)}^{(PC)} - A_{(12)}^{(PC)} Z^{(DEV)} A_{(22)}^{(PC)}^{-1}A_{(21)}^{(PC)} \). The result of the conventional method using ideal open/short-TEG is plotted with dot-dashed curves in Fig.4, and they almost agree with that of the conventional method. It means that the open and short-TEG were working almost ideally, and the primary error factor is identified to be the equivalent circuit approximation of the parasitic circuit. Figure 5 shows the result of numerical simulation of de-embedding when \( \sigma = 10 \)S/m, which suppose the loss of Si CMOS substrate. The accuracy of the proposed de-embedding method is stable and acceptable while that of the conventional one is neither stable nor accurate. The primary error factor is identified to be the equivalent circuit approximation of the parasitic circuit in this case, too.

4. Conclusion

The proposed de-embedding method using EM simulator is numerically simulated for an FET-TEG structure. The accuracy of conventional de-embedding method using open/short pattern is lower, especially in high frequency band, than the proposed method. The accuracy of the proposed de-embedding method is stable and acceptable while that of the conventional one is neither stable nor accurate in lossy substrate. The error of the conventional method is investigated, and it is found that the approximation of parasitic circuit by the equivalent circuit model is the primary error factor.
Acknowledgments

This work was partly supported by “The research and development project for expansion of radio spectrum resources” of The Ministry of Internal Affairs and Communications, Japan.

Figure 1: De-embedding Method Using EM Simulator

(1) Device with parasitic circuit

(2) Analyze S parameters of four port parasitic circuit

(3) Measure S-parameters of Open/Short patterns

(4) Device characteristic is calculated using S parameters in (2) and (3)

Figure 2: Structure of TEG

(a) FET-TEG

(b) Open-TEG

(c) Short-TEG

Figure 3: HFSS Analysis Models

(a) Model for Parasitic Circuit

(b) Model for Simulation of Measurement
References