Radio-frequency identification (RFID) technology emerges in recent years for its merits to collect information from a large number of assets quickly, easily and without human error. Contents of RFID tags can be read and/or modified without line-of-sight contact. While active tags need a battery to power the circuits, passive tags, on the other hand, do not need power supply and are more often used in large volume. The passive tag can be powered by rectifying the incoming energy to dc form. The energy source can be an RF signal received from antenna or a low-frequency (tens of kHz to several tens of MHz) ac signal collected via a coupling mechanism, for example, a magnetic coupler.

Ripple Stabilizer. An ideal voltage regulator is supposed to maintain a constant dc voltage independent of the amount of power received by the antenna and the power consumed by the tag. Such regulator is required to consume power less than a few tens of $\mu$W, and its temperature coefficient is preferred to be zero at room temperature. Fig. 1 shows the ripple stabilizer used in this regulator design. In order to provide a supply-independent reference current, the structure of cascode current mirror is adopted. The current mirror consists of four PMOSs, $M_1$, $M_2$, $M_3$, and $M_4$. The current $I_2$ follows $I_1$ closely if $M_1$ and $M_3$ match $M_2$ and $M_4$, respectively. On the other hand, the NMOS-based current mirror, $M_5$-$M_8$, make
$I_1$ follow $I_2$ if $M_5$ and $M_7$ matches $M_6$ and $M_8$, respectively. Since each diode-like pair ($M_1$ and $M_3$, $M_6$ and $M_8$) is fed by a constant-current source, $I_1$ and $I_2$ are relatively independence of $V_{DD}$. The cascode of $M_5$ and $M_7$ increases the output impedance observed by the diode-like pair $M_1$ and $M_3$, hence the reference current becomes less sensitive to the ripple voltage in $V_{DD}$.

**Temperature Stabilizer.** Fig. 2 shows the bandgap reference generator used in

![Schematic of bandgap reference generator](image)

Figure 2: Schematic of bandgap reference generator, (a) zero-TC voltage reference, (b) $\Delta V_{BE}$ generation circuit.

this design, a $\Delta V_{BE}$ generation is shown in Fig. 2(b). As shown in Fig. 2(a), this design superimposes $\Delta V_{BE}$ which exhibits a positive TC on $V_{EB}$ which exhibits a negative TC. Thus, $V_{REF}$ can be expressed as

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) \Delta V_{BE} + V_{EB}$$

and

$$\frac{\partial V_{REF}}{\partial T} = \left(1 + \frac{R_1}{R_2}\right) \frac{\kappa}{q} \ln n + \frac{V_{BE} - (4 + m)V_T - E_g/q}{T}$$

If $R_1/R_2 = 24$ and $n = 2$, the derivative of $V_{REF}$ with respect to $T$ approaches zero around $T = 300$ K, which implies that the reference voltage $V_{REF}$ is insensitive to temperature variation.

**Complete Circuit.** Fig. 3 shows the schematic of the proposed regulator, in which $I_{reg}$ is insensitive to voltage ripple as described. Also, $V_{REF}$ is insensitive to either ripple voltage or temperature variation, making it a stable reference for the operational amplifier.

The ripple stabilizer, temperature stabilizer, and operational amplifier are all designed with a cascode current mirror so that voltage ripple in $V_{DD}$ will induce negligible current variation. $R_L$ and $C_L$ represent the load from the subsequent stage, and
Figure 3: Schematic of proposed regulator. TS: temperature stabilizer, RS: ripple stabilizer, FVR: fixed voltage reference, OPA: operational amplifier.

$V_S$ is the regulated supply voltage. The ratio of $R_3/R_4$ is chosen so that $V_X \simeq V_{REF}$, large $W/L$ ratio of $M_{pass}$ is required to provide sufficient load current.

Considering a $V_{ripple}$ of sinusoidal waveform appearing on $V_{DD}$, current on $M_{pass}$ will be increased during the positive half period of $V_{ripple}$, hence pulling $V_S$ and $V_X$ up. The voltage increase of $V_X$ will activate the OPA to increase the voltage $V_F$, hence decreasing the conducting current of $M_{pass}$. Thus, $V_S$ will be brought back to its original dc level. On the other hand, the negative half period of $V_{ripple}$ causes a voltage drop at $V_S$ and $V_X$, the voltage decrease of $V_X$ will activate the OPA to decrease the voltage $V_F$, hence increasing the conducting current of $M_{pass}$. Since $V_{REF}$ is insensitive to ripple voltage and temperature variation, the regulated voltage $V_S$ is also insensitive to voltage ripple and temperature variation.

**Results and Discussions**

The quality of a regulator is conventionally measured in terms of line regulation (LIR), load regulation (LOR), and power supply ripple rejection (PSRR) defined as

$$LIR = \frac{\Delta V_o}{\Delta V_{DD}}$$

$$LOR = \frac{\Delta V_o}{\Delta I_L}$$

$$PSRR = 20 \log \frac{\Delta V_{DD}}{\Delta V_o}$$
Fig. 4(a) shows the output waveform $V_S$ given a variation in $V_{DD}$ of about 10 mV in magnitude, varying at 1 MHz. The dropout voltage is about 750 mV, the output voltage $V_S$ is about 1.8 V and the LIR is about 12 mV/V, which means $V_S$ is insensitive to the voltage ripple. Fig.4(b) shows the temperature variation of $V_{REF}$.

![Figure 4: Simulate results of (a) voltage swing of $V_S$ given a variation in $V_{DD}$ of about 10 mV in magnitude, varying at 1 MHz, (b) temperature variation of $V_{REF}$.](image)

References


